IN THE CLAIMS

1. (Original) A nonplanar semiconductor device comprising:

a semiconductor body having a top surface opposite a bottom surface formed above an insulating substrate, wherein said semiconductor body has a pair of laterally opposite sidewalls;

a gate dielectric formed on said top surface of said semiconductor body, on said bottom surface of said semiconductor body, and on said laterally opposite sidewalls of said semiconductor body;

a gate electrode formed on said gate dielectric, on said top surface of said semiconductor body and adjacent to said gate dielectric on said laterally opposite sidewalls of said semiconductor body and beneath said gate dielectric on said bottom surface of said semiconductor body; and

a pair of source/drain regions formed in said semiconductor body on opposite sides of said gate electrode.

2. (Original) The semiconductor device of claim 1 wherein said semiconductor body is a single crystalline silicon film.

3. (Original) The semiconductor device of claim 1 wherein said semiconductor body is selected from the group consisting of germanium, silicon germanium, gallium arsenide, InSb, GaP, GaSb and carbon nanotubes.

4. (Original) The semiconductor device of claim 1 wherein said gate electrode comprises a material selected from the group consisting of polycrystalline silicon, tungsten, tantalum, titanium, and metal nitrides.

5. (Original) The semiconductor device of claim 1 wherein said insulating substrate comprises an oxide film formed on a monocrystalline silicon substrate.

6. (Original) The semiconductor device of claim 1 wherein said semiconductor device further includes at least one additional semiconductor body having a top surface and a bottom surface, and a pair of laterally opposite sidewalls wherein a gate dielectric layer is formed said top surface, said bottom surface and said sidewalls of said at least one other semiconductor body, and wherein said gate electrode is formed on said gate dielectric on said top surface of said at least one other semiconductor body, and adjacent to said gate dielectric on said laterally opposite sidewalls of said at least one other semiconductor body, and beneath the gate dielectric on said bottom surface of said at least one other semiconductor body.

7. (Original) A nonplanar semiconductor device comprising:

a semiconductor body having a top surface opposite a bottom surface having a portion formed on an insulating substrate, said semiconductor body having laterally opposite sidewalls formed above said insulating substrate;

a gate dielectric formed on said top surface of said semiconductor body, on said laterally opposite sidewalls of said semiconductor body, and on portion of the bottom surface of said semiconductor body not on said insulating substrate;

a gate electrode formed on said gate dielectric on said top surface of said semiconductor body and adjacent to said gate dielectric on said laterally opposite sidewalls of said semiconductor body, and beneath said gate dielectric on said bottom surface of said semiconductor body; and

a pair of source/drain regions formed in said silicon body on opposite sides of said gate electrode.

8. (Original) The semiconductor device of claim 7 wherein said semiconductor body is a single crystalline silicon film.

9. (Original) The semiconductor device of claim 7 wherein said semiconductor body is selected from the group consisting of germanium, silicon germanium, gallium arsenide, InSb, GaP, GaSb and carbon nanotubes.

10. (Original) The semiconductor device of claim 7 wherein said gate electrode comprises a material selected from the group consisting of polycrystalline silicon, tungsten, tantalum, titanium and metal nitrides.

11. (Original) The semiconductor device of claim 7 wherein said insulating substrate comprises an oxide film formed on a monocrystalline silicon substrate.

12. (Original) The semiconductor device of claim 1 wherein said semiconductor device further includes at least one additional semiconductor body having a top surface and a bottom surface, and a pair of laterally opposite sidewalls wherein a gate dielectric layer is formed said top surface, said bottom surface and said sidewalls of said at least one other semiconductor body, and wherein said gate electrode is formed on said gate dielectric on said top surface of said at least one other semiconductor body, and adjacent to said gate dielectric on said laterally opposite sidewalls of said at least one other semiconductor body, and beneath the gate dielectric on said bottom surface of said at least one other semiconductor body.

13. (Withdrawn) A method of forming a nonplanar semiconductor device comprising:

forming a semiconductor body having a top surface opposite a bottom surface and a pair of laterally opposite sidewalls above an insulating substrate;

forming a gate dielectric on said top surface of said semiconductor body, on said laterally opposite sidewalls of said semiconductor body, and on at least a portion of said bottom surface of said semiconductor body;

forming a gate electrode on said gate dielectric on said top surface of said semiconductor body and adjacent to said gate dielectric on said laterally opposite sidewalls of said semiconductor body and subadjacent to said gate dielectric formed on at least a portion of said bottom surface of said semiconductor body; and

forming a pair of source/drain regions in said semiconductor body on opposite sides of said gate electrode.

14. (Withdrawn) The method for forming said semiconductor device of claim 13 wherein said gate dielectric and gate electrode are formed beneath the entire channel region of said semiconductor body.

15. (Withdrawn) The method of claim 13 wherein a portion of the bottom surface of said semiconductor body is formed on said insulating substrate wherein said portion on said insulating substrate is located beneath said gate electrode above said top surface of said semiconductor body.

16. (Withdrawn) The method of claim 13 wherein said semiconductor body is a single crystalline silicon film.

17. (Withdrawn) The method of claim 13 wherein said semiconductor body is selected from the group consisting of germanium, silicon germanium, gallium arsenide, InSb, GaP, GaSb and carbon nanotubes.

18. (Withdrawn) The method of claim 13 wherein said gate electrode comprises a material selected from the group consisting of polycrystalline silicon, tungsten, tantalum, titanium and metal nitrides.

19. (Withdrawn) The method of claim 13 wherein said insulating substrate comprises an oxide film formed on a monocrystalline silicon substrate.

20. (Withdrawn) The method of claim 13 further including forming at least one additional semiconductor body having a top surface and a bottom surface, and a pair of laterally opposite sidewalls and forming a gate dielectric layer over said top surface, said bottom surface and said sidewalls of said at least one other semiconductor body, and wherein said gate electrode is formed on said gate dielectric on said top surface of said at least one other semiconductor body, and adjacent to said gate dielectric on said laterally opposite sidewalls of said at least one other semiconductor body, and beneath the gate dielectric on said bottom surface of said at least one other semiconductor body.

21. (Withdrawn) A method of forming a nonplanar transistor comprising:

forming a semiconductor body having a pair of laterally opposite sidewalls and a top surface and a bottom surface on an insulating substrate;

removing a portion of said insulating substrate from beneath said semiconductor body to undercut said semiconductor body and expose a portion of said bottom surface of said semiconductor body;

forming a gate dielectric on said top surface of said semiconductor body, on said sidewalls of said semiconductor body, and on said exposed bottom portion of said semiconductor body;

depositing a gate material over and around said semiconductor body and beneath said exposed portion of said semiconductor body;

etching gate electrode material into a gate electrode utilizing a first anisotropic etch followed by a isotropic etch to form a gate electrode which is formed over the gate dielectric layer on the top surface of said semiconductor body and is formed adjacent the gate dielectric formed on the sidewalls of said semiconductor body and is formed beneath said gate dielectric formed on said exposed portions of said bottom surface of said semiconductor body; and

placing dopants into said semiconductor body on opposite sides of said gate electrode to form a pair of source/drain regions.

22. (Withdrawn) The method of claim 21 wherein said semiconductor body is formed from single crystalline silicon.

23. (Withdrawn) The method of claim 22 wherein said insulating substrate comprises a lower monocrystalline silicon substrate and a top silicon oxide,

24. (Withdrawn) A method of forming a nonplanar transistor comprising:

forming a semiconductor body having a top surface and a bottom surface and a pair of laterally opposite sidewalls on an insulating substrate;

forming a dielectric film over and around said semiconductor body, wherein said dielectric film has an opening which exposes the channel region of said semiconductor body;

removing a portion of said insulating substrate in said opening beneath said semiconductor body to expose at least a portion of said bottom surface of said semiconductor body;

forming a gate dielectric layer on said top surface and said sidewalls of said semiconductor body in said opening and on said exposed portion of said bottom surface of said semiconductor body;

blanket depositing a gate electrode material over said dielectric film and into said opening and on said gate dielectric layer on said top surface of said semiconductor body, adjacent to said gate dielectric on said sidewalls of said semiconductor body and beneath said gate dielectric on said exposed portions of said semiconductor body;

removing said gate electrode material from the top surface of said dielectric film to form a gate electrode;

removing said dielectric film; and

placing dopants into said semiconductor body on opposite sides of said electrode to form a pair source/drain regions.

25. (Withdrawn) The method of claim 24 wherein said semiconductor body is formed from single crystalline silicon.

26. (Withdrawn) The method of claim 25 wherein said insulating substrate comprises a lower monocrystalline silicon substrate and a top silicon oxide insulating film.

27. (Withdrawn) A method of forming a nonplanar transistor comprising:

forming a semiconductor body having a top surface and bottom surface and a pair of laterally opposite sidewalls on an insulating substrate;

forming a sacrificial gate electrode above said top surface of said semiconductor body and adjacent to said laterally opposite sidewalls of said semiconductor body, said sacrificial gate electrode having a pair of laterally opposite sidewalls;

placing dopants into said semiconductor body on opposite sides of said sacrificial gate electrode to form a pair of source/drain extensions on opposite sides of said gate electrode;

forming a pair of sidewall spacers along laterally opposite sidewalls of said sacrificial gate electrode;

forming silicon on said semiconductor body adjacent to said sidewall spacers;

placing dopants into said silicon and into said semiconductor body in alignment with said sidewall spacers;

forming a silicide on said silicon formed on said semiconductor body adjacent to said sidewall spacers;

forming a dielectric layer over said silicide, said sacrificial gate electrode and said sidewall spacers;

planarizing said dielectric layer until the top surface of said dielectric layer is planar with the top surface of said sacrificial gate electrode and said sacrificial gate electrode is exposed;

removing said sacrificial gate electrode to expose the channel region of said semiconductor body and said insulating substrate;

removing a portion of said insulating substrate in said opening beneath said semiconductor body to expose at least a portion of said bottom surface of said semiconductor body;

forming a gate dielectric layer on said top surface and said sidewalls of said semiconductor body in said opening and on said portion of said exposed bottom surface of said semiconductor body;

blanket depositing a gate electrode material on said gate dielectric layer and into said opening and on said gate dielectric layer on said top surface of said semiconductor body, adjacent to said gate dielectric on said sidewalls of said semiconductor body, and beneath said gate dielectric on said exposed portion of said bottom surface of said semiconductor body; and

removing said gate electrode material from the top surface of said dielectric film to form a gate electrode.

28. (Withdrawn) The method of claim 27 wherein semiconductor body is formed from single crystalline silicon.

29. (Withdrawn) The method of claim 28 wherein said insulating substrate comprises a lower monocrystalline silicon substrate and a top silicon insulating film.